AMENDMENTS TO THE CLAIMS

Please amend Claims 16, 20, 25, 26, and 31 of the Application as follows, and cancel Claims 23 and 24 of the Application, without prejudice or disclaimer to continued examination on the merits:

16. (currently amended) A rearrangeable, non-blocking switch, comprising:

a first stage including a plurality of first switch circuits, each of said plurality of first switch circuits including a plurality of inputs and a plurality of outputs;

a second stage including a plurality of second switch circuits, each of said plurality of second switch circuits including a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2; and

a third stage including a plurality of third switch circuits, each of said plurality of third switch circuits including a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits,

wherein at least some of said plurality of second switch circuits are each configured as a plurality of logical switch circuits, wherein a Looping Algorithm is used as a control algorithm for the switch, and

wherein each of said plurality of outputs of said plurality of first switch circuits outputs a respective one of a plurality of data signals, said data signals being multiplexed, wherein said each of said plurality of data signals includes a plurality of groups, each of said plurality of groups further including a plurality of subgroups.

17. (previously presented) A switch in accordance with claim 16, wherein at least one of the plurality of logical switch circuits does not carry data in order to configure the

at least some of said plurality of second switch circuits as n logical switch circuits, where n is a power of 2.

18. (canceled)

19. (previously presented) A switch in accordance with claim 16, wherein each of said plurality of first and third switch circuits are configured to be logically represented as respective groupings of 2 x 2 switches.

20. (currently amended) A switch in accordance with claim 16, wherein each of said plurality of outputs of said plurality of first switch circuits, outputs a respective one of a plurality of data signals, said data signals being time-division multiplexed.

21. (previously presented) A switch in accordance with claim 20, wherein each of said plurality of data signals includes a plurality of groups of time slots, each of said plurality of groups of time slots further including a plurality of subgroups of time slots.

22. (previously presented) A switch in accordance with claim 16,

wherein a number of said first switch circuits is 32 and said first switch circuits have a total of 384 inputs each,

wherein the number N of said second switch circuits is 22, and

wherein a number of said third switch circuits is 32 and said third switch circuits have a total of 384 outputs each.

23. (canceled)

24. (canceled)

25. (currently amended) A rearrangeable, non-blocking, three-stage switch configured as a Clos network, said switch comprising:

a plurality of physical center stage switch circuits, a number of said plurality of physical center stage switch circuits equaling N, where N is an integer other than a power of 2;

a plurality of logical center stage switch circuits equaling N*f, where f is a number of logical center stage switch circuits per physical center stage switch circuit, wherein the plurality of physical center stage switch circuits are configured into the plurality of logical center stage switch circuits; and

a subset of the plurality of logical center stage switch circuits equaling n, where n is less than N*f and n is a power of 2,

wherein a plurality of inputs of said plurality of logical center stage switch circuits inputs a respective one of a plurality of data signals, said data signals being multiplexed, wherein said each of said plurality of data signals includes a plurality of groups, each of said plurality of groups further including a plurality of subgroups.

26. (currently amended) The switch of claim 25, wherein the subset of the plurality of logical center stage switch circuits initially carries no data signals and ~~may be~~ is listed as spares.

27-30. (canceled)

31. (currently amended) The switch of claim 25, wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch.

32. (canceled)

33. (canceled)

34. (previously presented) The switch of claim 25, wherein a looping algorithm is used as a control algorithm for the switch.